

TPS3705-30, TPS3705-33, TPS3705-50  
 TPS3707-25, TPS3707-30, TPS3707-33, TPS3707-50  
 PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL

SLVS184B – NOVEMBER 1998 – REVISED JANUARY 1999

features

- Power-On Reset Generator with Fixed Delay Time of 200 ms, no External Capacitor Needed
- Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, and 5 V
- Pin-For-Pin Compatible with the MAX705 through MAX708 Series
- Integrated Watchdog Timer (TPS3705 only)
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Maximum Supply Current of 50  $\mu$ A
- MSOP-8 and SO-8 Packages
- Temperature Range . . .  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

typical applications

- Designs Using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

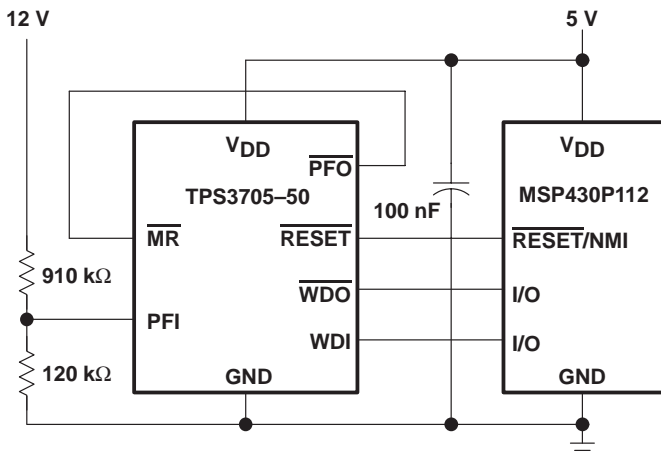
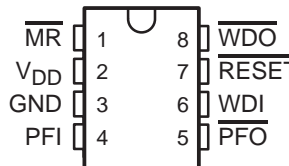
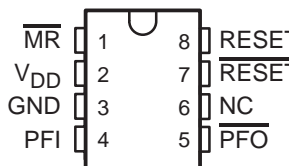


Figure 1. Typical MSP430 Application

TPS3705 . . . D PACKAGE  
 (TOP VIEW)

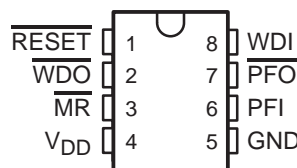


TPS3707 . . . D PACKAGE  
 (TOP VIEW)

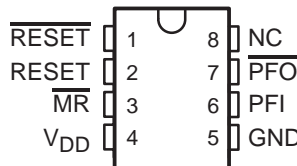


NC – No internal connection

TPS3705 . . . DGN PACKAGE  
 (TOP VIEW)



TPS3707 . . . DGN PACKAGE  
 (TOP VIEW)



NC – No internal connection



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**TPS3705-30, TPS3705-33, TPS3705-50**  
**TPS3707-25, TPS3707-30, TPS3707-33, TPS3707-50**  
**PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL**  
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**description**

The TPS3705, TPS3707 family of microprocessor supply-voltage supervisors provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{DD}$  becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors  $V_{DD}$  and keeps  $\overline{\text{RESET}}$  active as long as  $V_{DD}$  remains below the threshold voltage  $V_{IT+}$ . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{d\text{typ}} = 200$  ms, starts after  $V_{DD}$  has risen above the threshold voltage  $V_{IT+}$ . When the supply voltage drops below the threshold voltage  $V_{IT-}$ , the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage  $V_{IT-}$  set by an internal voltage divider.

The TPS3705-xx and TPS3707-xx devices incorporate a manual reset input,  $\overline{\text{MR}}$ . A low level at  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to become active.

The TPS370x-xx families integrate a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3705-xx devices have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval,  $t_{t(\text{out})} = 1.6$  s,  $\overline{\text{WDO}}$  becomes active. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3707-xx devices do not have the Watchdog function, but include a high-level output RESET.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in either 8-pin MSOP or standard SOIC packages. The TPS3705, TPS3707 devices are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**AVAILABLE OPTIONS**

T <sub>A</sub>	THRESHOLD VOLTAGE	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
		SMALL OUTLINE (D)	POWER-PAD™ μ-SMALL OUTLINE (DGN)		
-40°C to 85°C	2.63 V	TPS3705-30D	TPS3705-30DGN	TIAAT	TPS3705-30Y
	2.93 V	TPS3705-33D	TPS3705-33DGN	TIAAU	TPS3705-33Y
	4.55 V	TPS3705-50D	TPS3705-50DGN	TIAAV	TPS3705-50Y
	2.25 V	TPS3707-25D	TPS3707-25DGN	TIAAW	TPS3707-25Y
	2.63 V	TPS3707-30D	TPS3707-30DGN	TIAAX	TPS3707-30Y
	2.93 V	TPS3707-33D	TPS3707-33DGN	TIAAY	TPS3707-33Y
	4.55 V	TPS3707-50D	TPS3707-50DGN	TIAAZ	TPS3707-50Y



**Function Tables**

TRUTH TABLE, TPS3705

$\overline{\text{MR}}$	$V_{\text{DD}} > V_{\text{IT}}$	$\overline{\text{RESET}}$	TYPICAL DELAY
H→L	1	H→L	30 ns
L→H	1	L→H	200 ms
H	1→0	H→L	3 μs
H	0→1	L→H	200 ms

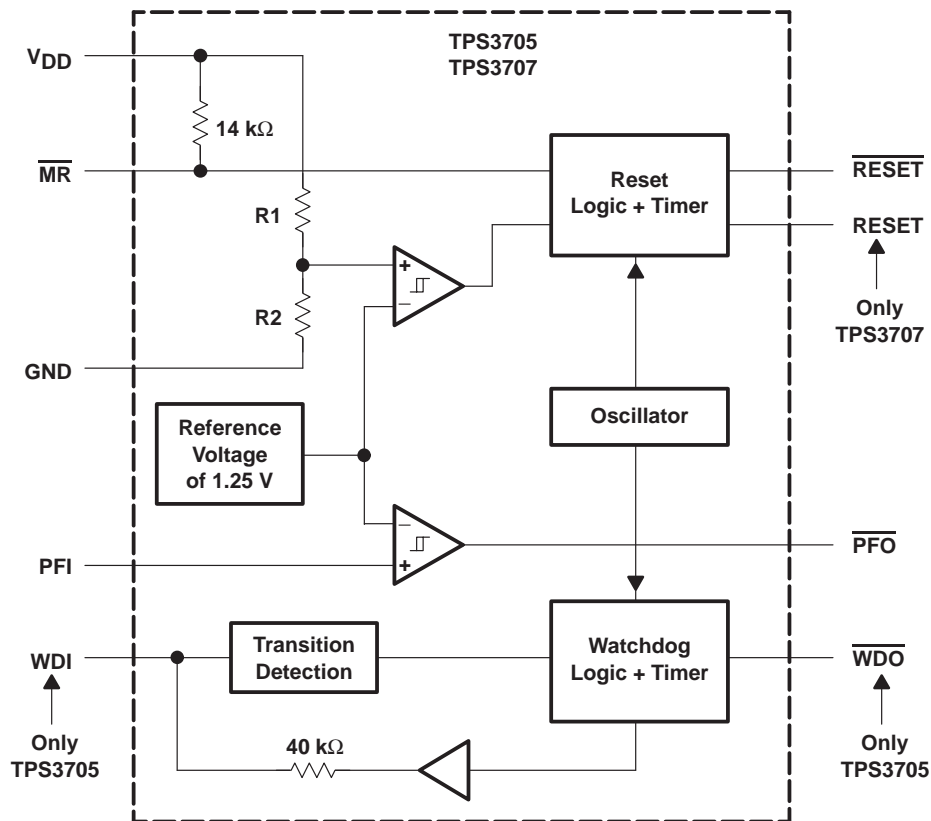
TRUTH TABLE, TPS3707

$\overline{\text{MR}}$	$V_{\text{DD}} > V_{\text{IT}}$	$\overline{\text{RESET}}$	RESET	TYPICAL DELAY
H→L	1	H→L	L→H	30 ns
L→H	1	L→H	H→L	200 ms
H	1→0	H→L	L→H	3 μs
H	0→1	L→H	H→L	200 ms

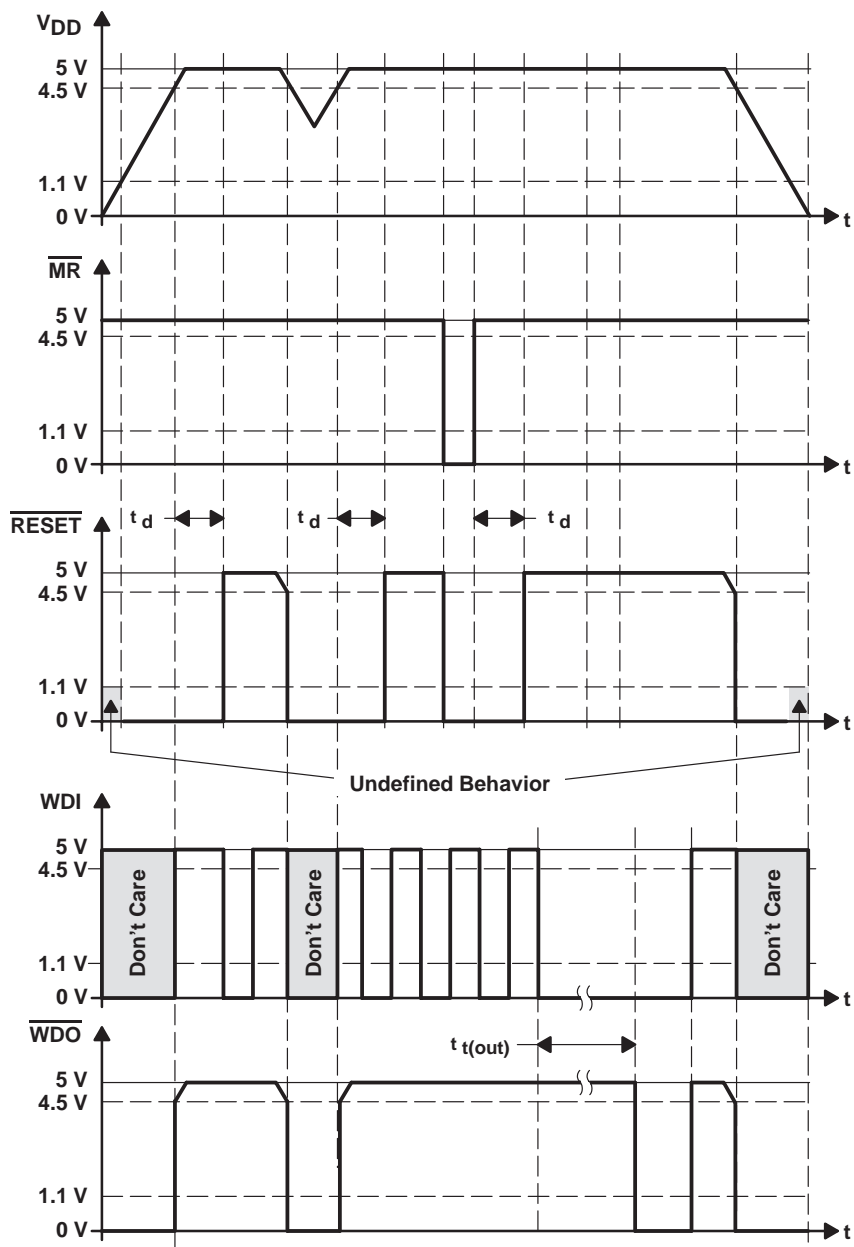
TRUTH TABLE, TPS370x

$\text{PFI} > V_{\text{IT}}$	$\overline{\text{PFO}}$	TYPICAL DELAY
0→1	L→H	0.5 μs
1→0	H→L	0.5 μs

**functional block diagram**



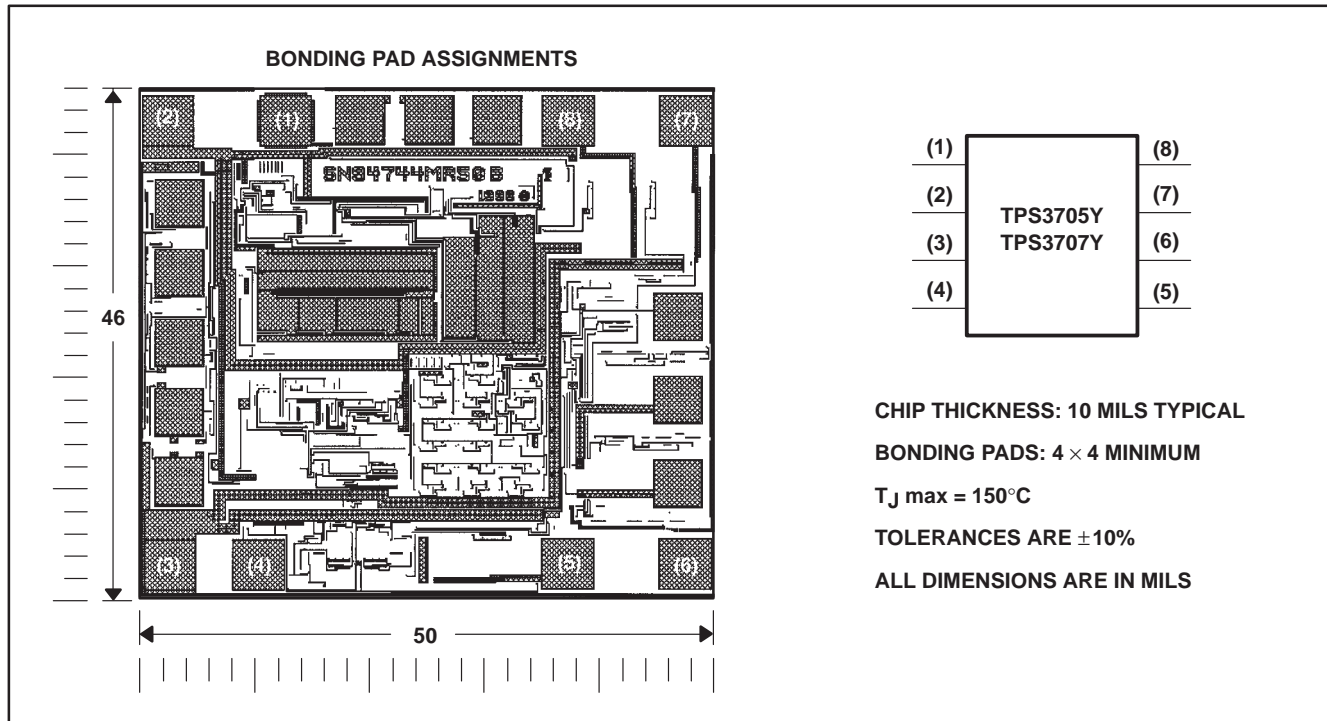
timing diagrams



TPS3705-30, TPS3705-33, TPS3705-50  
 TPS3707-25, TPS3707-30, TPS3707-33, TPS3707-50  
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**TPS370xY chip information**

These chips, when properly assembled, display characteristics similar to those of the TPS370x. Thermal compression or ultrasonic bonding may be caused on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



**Terminal Functions**

TERMINAL NAME		NO.	I/O	DESCRIPTION
MR		1	I	Manual reset
VDD		2		Supply voltage
GND		3		Ground
PFI		4	I	Power-fail comparator input
PFO		5	O	Power-fail comparator output
WDI	TPS3705	6	I	Watchdog timer input
NC	TPS3707			No internal connection
RESET		7	O	Active-low reset output
WDO	TPS3705	8	O	Watchdog timer output
RESET	TPS3707			Active-high reset output

**TPS3705-30, TPS3705-33, TPS3705-50**  
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**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage, $V_{DD}$ (see Note1) .....	7 V
All other pins (see Note 1) .....	-0.3 V to 7 V
Maximum low output current, $I_{OL}$ .....	5 mA
Maximum high output current, $I_{OH}$ .....	-5 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ ) .....	$\pm 20$ mA
Continuous total power dissipation .....	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ .....	-40°C to 85°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C
Soldering temperature .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than  $t = 1000h$  continuously.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W
D	725 mW	5.8 mW/°C	464 mW	377 mW

**recommended operating conditions at specified temperature range**

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$	2	6	V
Input voltage, $V_I$	0	$V_{DD}+0.3$	V
High-level input voltage, $V_{IH}$	$0.7 \times V_{DD}$		V
Low-level input voltage, $V_{IL}$	$0.3 \times V_{DD}$		V
Input transition rise and fall rate at $\overline{MR}$ or $WDI$ , $\Delta t/\Delta V$	100		ns/V
Operating free-air temperature range, $T_A$	-40	85	°C



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT						
V <sub>OH</sub>	High-level output voltage	TPS370x-xx	V <sub>DD</sub> = 1.1 V, I <sub>OH</sub> = -4 μA	0.8			V						
		TPS3707-25	V <sub>DD</sub> = V <sub>IT+</sub> + 0.2 V, I <sub>OH</sub> = -500 μA	0.7 × V <sub>DD</sub>									
		TPS370x-30											
		TPS370x-33											
		TPS370x-50	V <sub>DD</sub> = V <sub>IT+</sub> + 0.2 V, I <sub>OH</sub> = -800 μA	V <sub>DD</sub> - 1.5 V									
TPS370x-xx	V <sub>DD</sub> = 6 V, I <sub>OH</sub> = -800 μA												
V <sub>OL</sub>	Low-level output voltage	TPS3707-25	V <sub>DD</sub> = V <sub>IT+</sub> + 0.2 V, I <sub>OL</sub> = 1 mA	0.3			V						
		TPS370x-30											
		TPS370x-33											
		TPS370x-50	V <sub>DD</sub> = V <sub>IT+</sub> + 0.2 V, I <sub>OL</sub> = 2.5 mA	0.4			V						
		TPS370x-xx	V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 3 mA										
Power-up reset voltage (see Note 2)		V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 50 μA	0.3			V							
V <sub>IT-</sub>	Negative-going input threshold voltage (see Note 3)	PFI	TPS370x-xx	V <sub>DD</sub> ≥ 2 V, T <sub>A</sub> = -40°C to 85°C	1.20	1.25	1.30	V					
					V <sub>DD</sub>	TPS3707-25	T <sub>A</sub> = 0°C to 85°C		2.20	2.25	2.30	V	
									TPS370x-30	2.57	2.63		2.68
									TPS370x-33	2.87	2.93		2.98
		TPS370x-50	4.45	4.55				4.63					
		V <sub>DD</sub>	TPS3707-25	T <sub>A</sub> = -40°C to 85°C	2.20	2.25	2.32	V					
					TPS370x-30	2.57	2.63		2.70				
					TPS370x-33	2.87	2.93		3.0				
					TPS370x-50	4.45	4.55		4.65				
		V <sub>hys</sub>	Hysteresis	V <sub>DD</sub>	TPS370x-xx	V <sub>DD</sub> ≥ 2 V, T <sub>A</sub> = -40°C to 85°C	40			mV			
50													
50													
70													
PFI	TPS370x-xx				10								
I <sub>IH(AV)</sub>	Average high-level input current	WDI		W <sub>DI</sub> = V <sub>DD</sub> = 6 V, Time average (dc = 88%)	100	150	μA						
I <sub>IL(AV)</sub>	Average low-level input current				W <sub>DI</sub> = 0 V, V <sub>DD</sub> = 6 V, Time average (dc = 12%)	-15	-20	μA					
I <sub>IH</sub>	High-level input current	WDI		W <sub>DI</sub> = V <sub>DD</sub> = 6 V	120	170	μA						
		MR			MR = 0.7 × V <sub>DD</sub> , V <sub>DD</sub> = 6 V	-130		-180					
I <sub>IL</sub>	Low-level input current	WDI		W <sub>DI</sub> = 0 V, V <sub>DD</sub> = 6 V	-120	-170	μA						
		MR			MR = 0 V, V <sub>DD</sub> = 6 V	-430		-600					
I <sub>I</sub>	Input current	PFI		V <sub>DD</sub> = 6 V, 0 V ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	-1	0	1	μA					
I <sub>DD</sub>	Supply current	TPS3707-xx		V <sub>DD</sub> = 2 V to 6 V, MR = V <sub>DD</sub> , MR, W <sub>DI</sub> and outputs unconnected	20	50	μA						
		TPS3705-xx		V <sub>DD</sub> = 2 V to 6 V, MR = V <sub>DD</sub> , MR, W <sub>DI</sub> and outputs unconnected	30	50	μA						
C <sub>i</sub>	Input capacitance			V <sub>I</sub> = 0 V to V <sub>DD</sub>	5		pF						

NOTES: 2. The lowest supply voltage at which RESET becomes active. t<sub>r,VDD</sub> ≥ 15 μs/V  
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near to the supply terminals.



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timing requirements at  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_w$	Pulse width					
	at $V_{DD}$	$V_{DD} = V_{IT+} + 0.2\text{ V}$ , $V_{DD} = V_{IT-} - 0.2\text{ V}$	6			$\mu\text{s}$
	at $\overline{\text{MR}}$	$V_{DD} \geq V_{IT+} + 0.2\text{ V}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$	100			ns
	at $\text{WDI}$	$V_{DD} \geq V_{IT+} + 0.2\text{ V}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$	100			ns

switching characteristics at  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out	$V_{DD} \geq V_{IT+} + 0.2\text{ V}$ , See timing diagram	1.1	1.6	2.3	s
$t_d$	Delay time	$V_{DD} > V_{IT+} + 0.2\text{ V}$ , See timing diagram	140	200	280	ms
$t_{PHL}$	Propagation (delay) time, high-to-low-level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ delay		50	250	ns
$t_{PLH}$	Propagation (delay) time, low-to-high-level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ delay (TPS3707-xx only)		50	250	
$t_{PHL}$	Propagation (delay) time, high-to-low-level output	$V_{DD}$ to $\overline{\text{RESET}}$ delay		3	5	$\mu\text{s}$
$t_{PLH}$	Propagation (delay) time, low-to-high-level output	$V_{DD}$ to $\overline{\text{RESET}}$ delay (TPS3707-xx only)		3	5	
$t_{PHL}$	Propagation (delay) time, high-to-low-level output	PFI to $\overline{\text{PFO}}$ delay	$V_{DD} = 2\text{ V to }6\text{ V}$	0.5	1	$\mu\text{s}$
$t_{PLH}$	Propagation (delay) time, low-to-high-level output			0.5	1	





TYPICAL CHARACTERISTICS

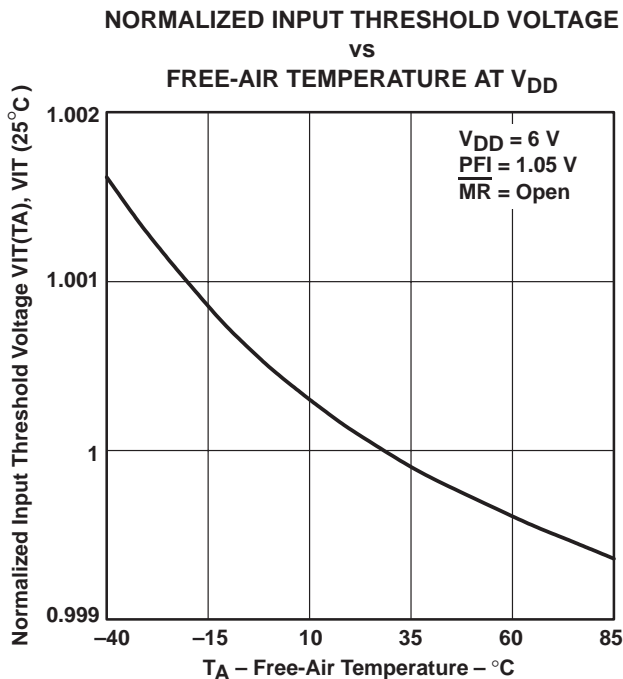


Figure 2

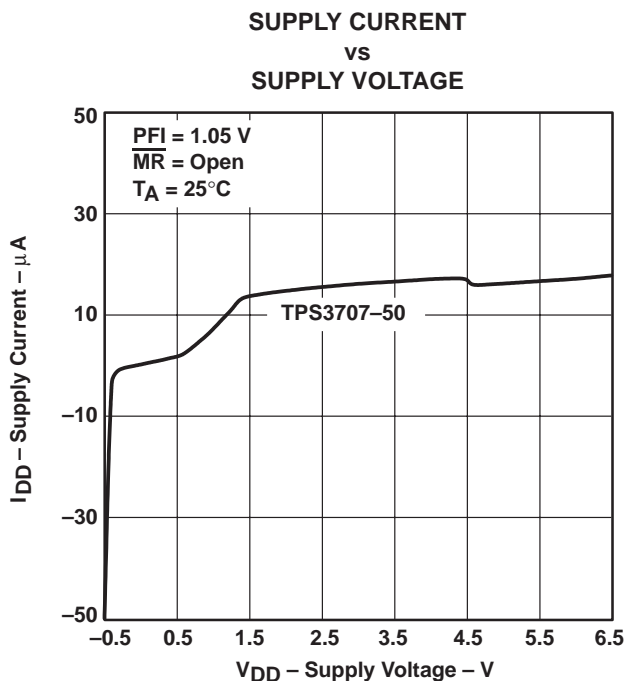


Figure 3

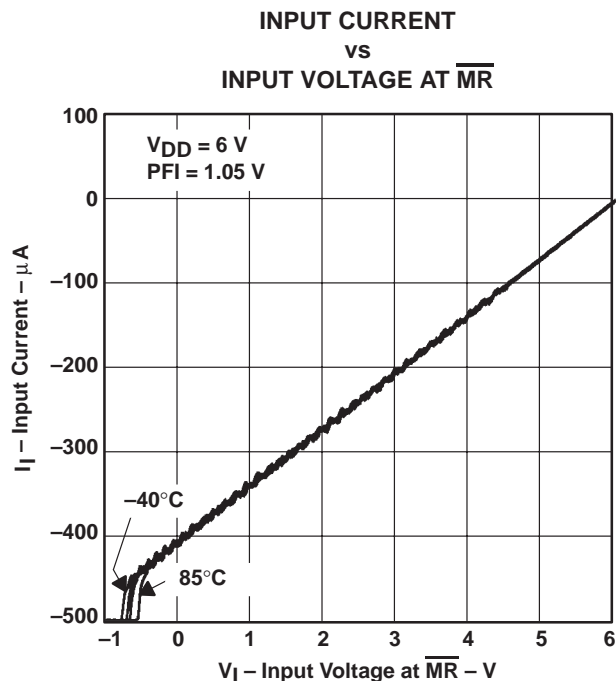


Figure 4

TYPICAL CHARACTERISTICS

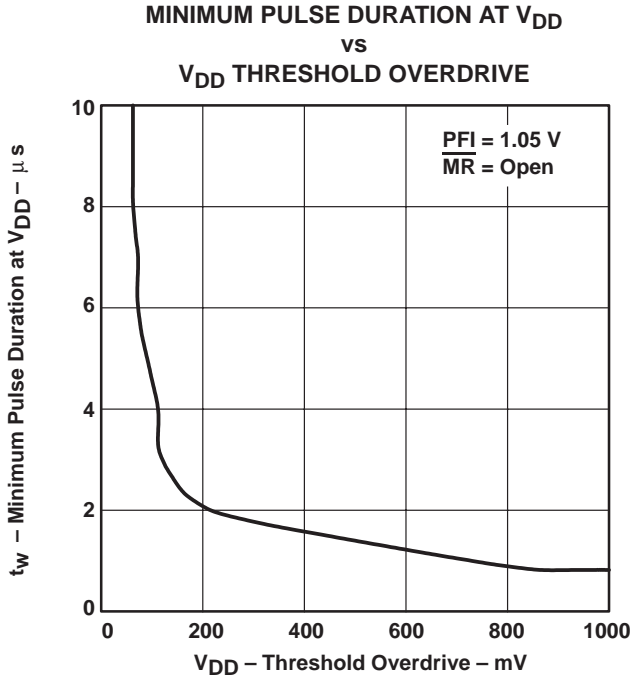


Figure 5

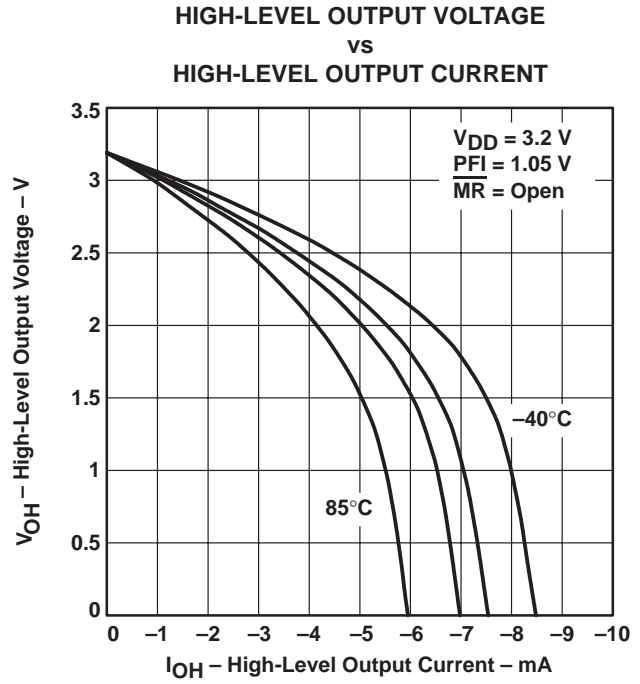


Figure 6

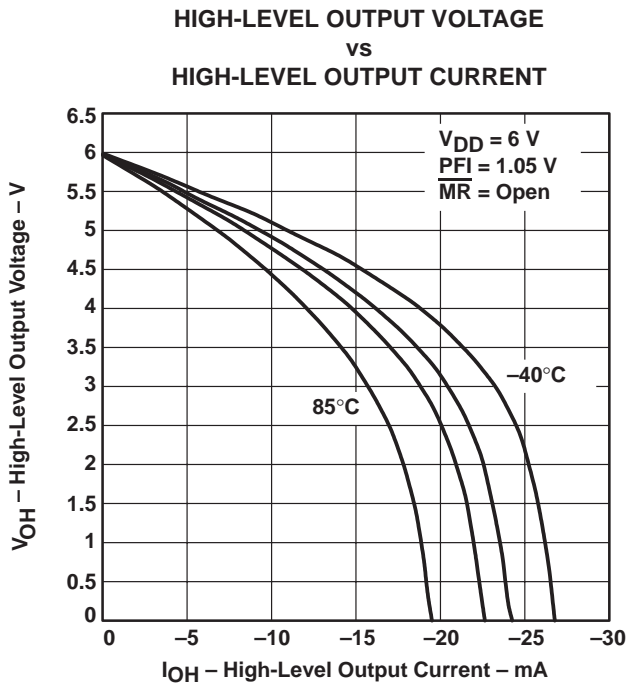


Figure 7

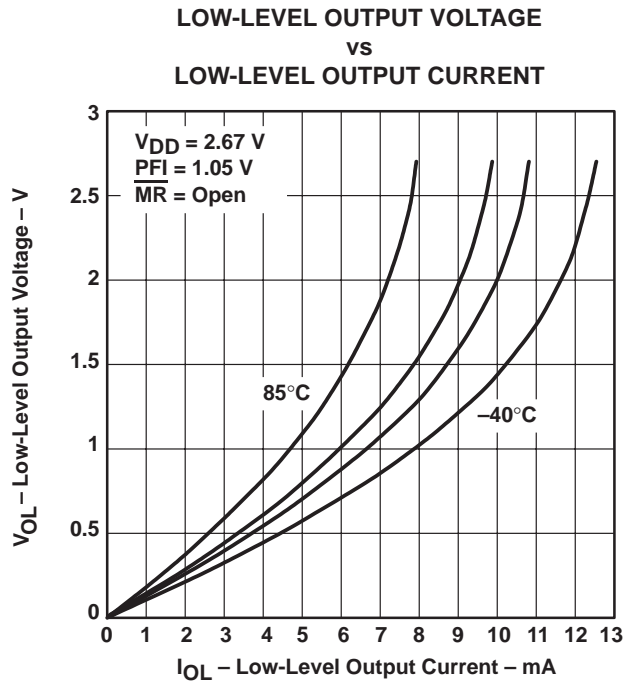


Figure 8

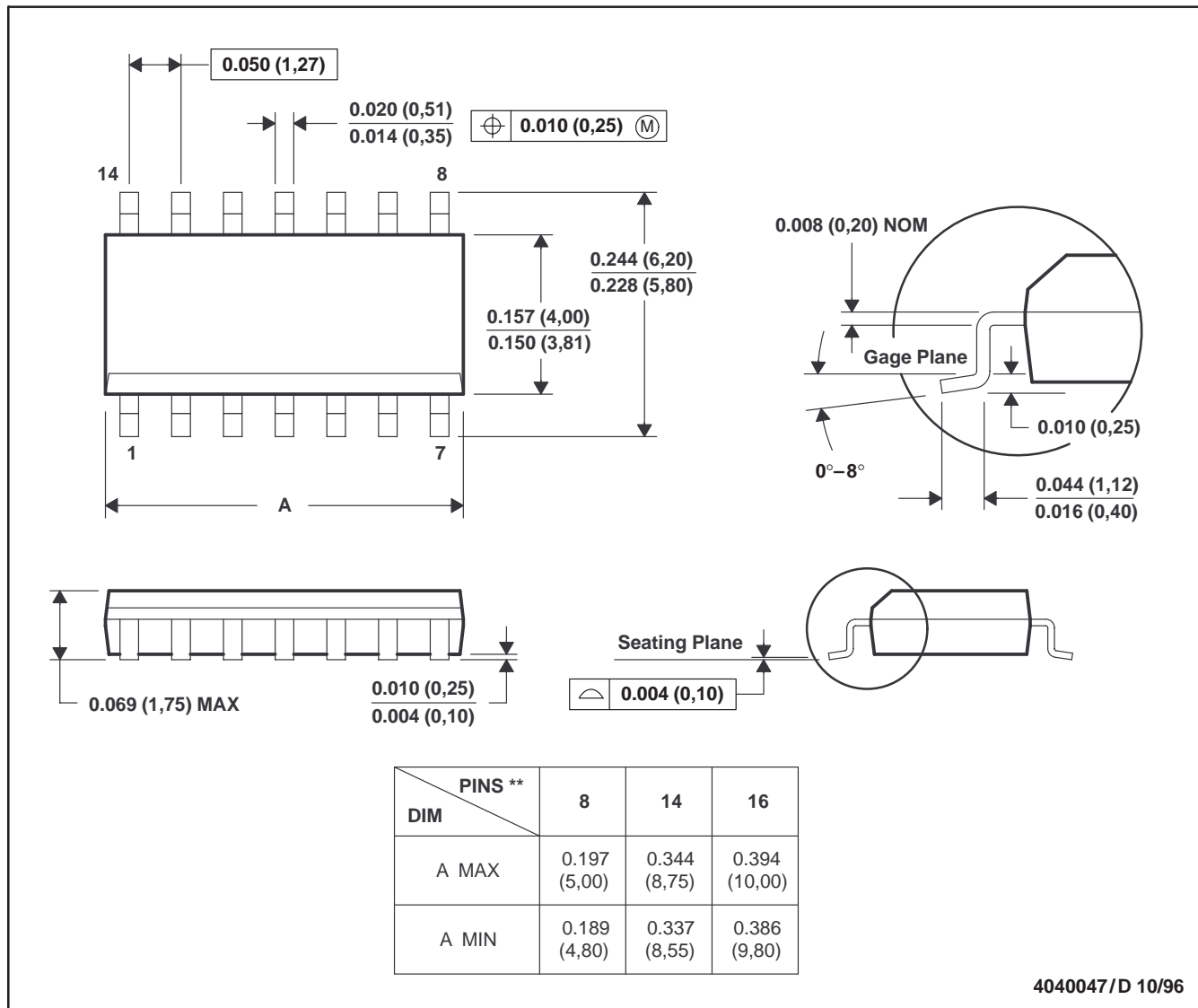
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MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



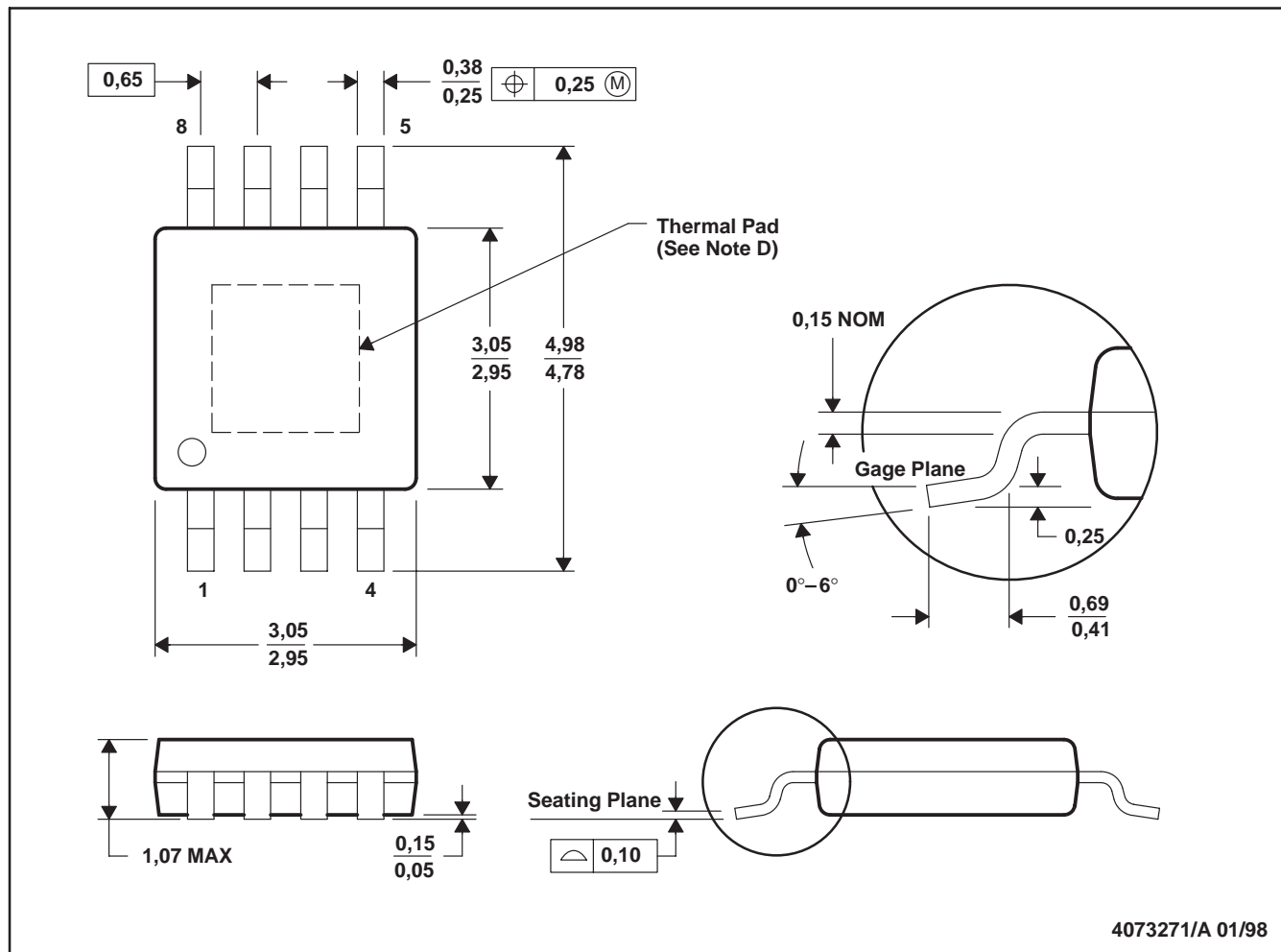
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

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MECHANICAL DATA

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



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 B. This drawing is subject to change without notice.  
 C. Body dimensions include mold flash or protrusions.  
 D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.  
 E. Falls within JEDEC MO-187

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